

Figure 1(a)

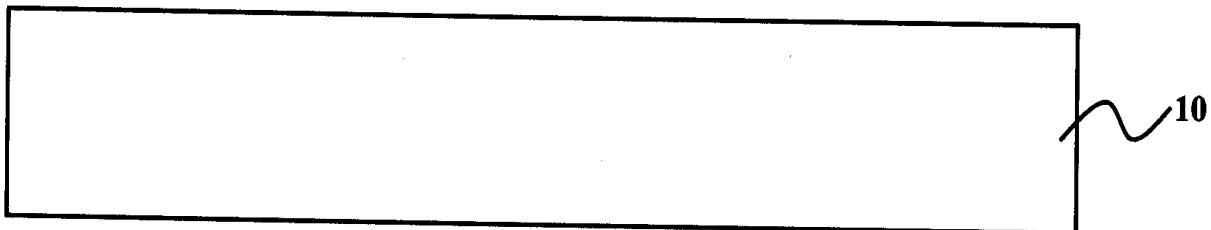


Figure 1(b)

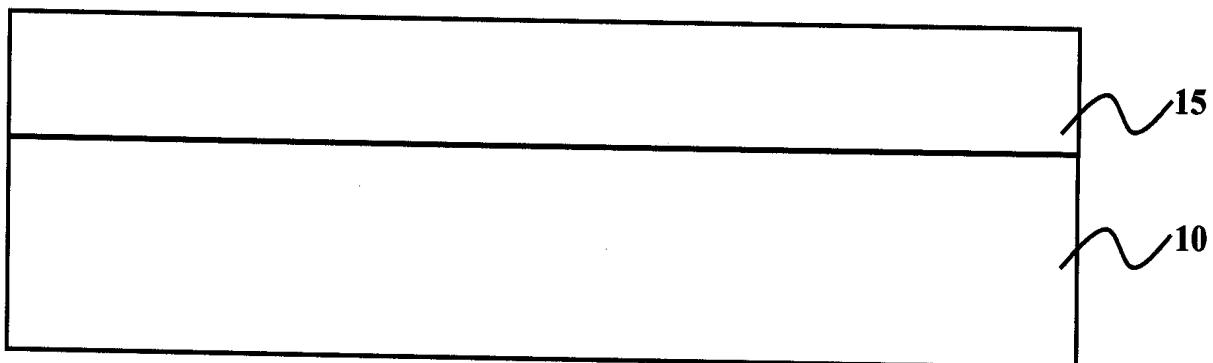


Figure 1(c)

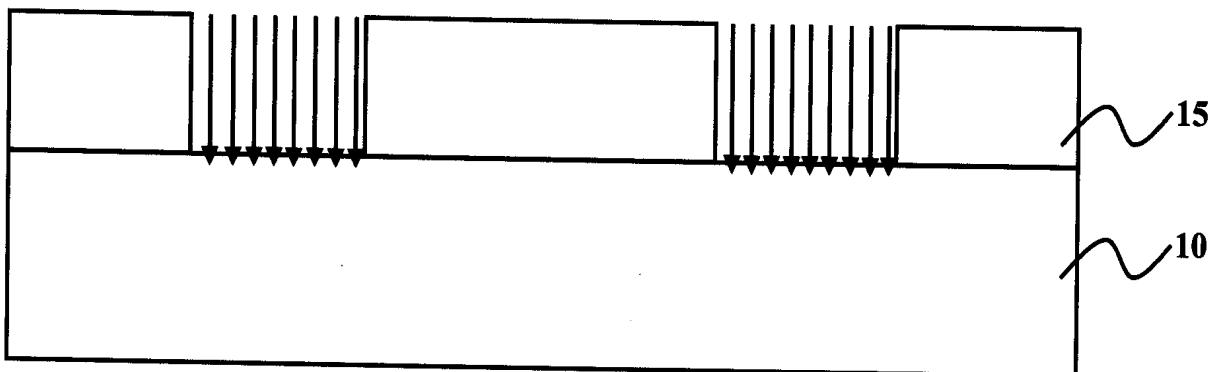


Figure 1(d)

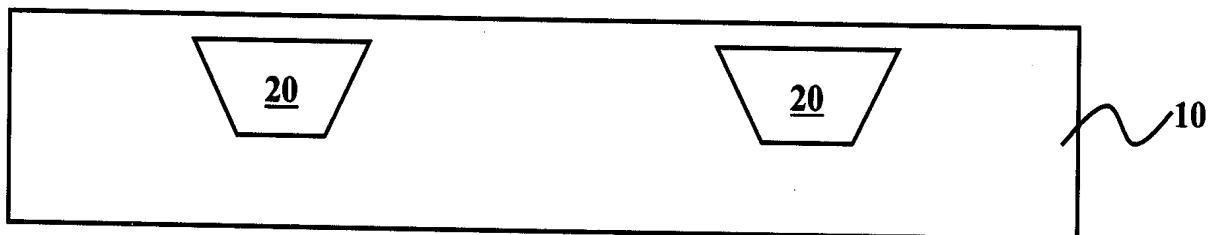


Figure 1(e)

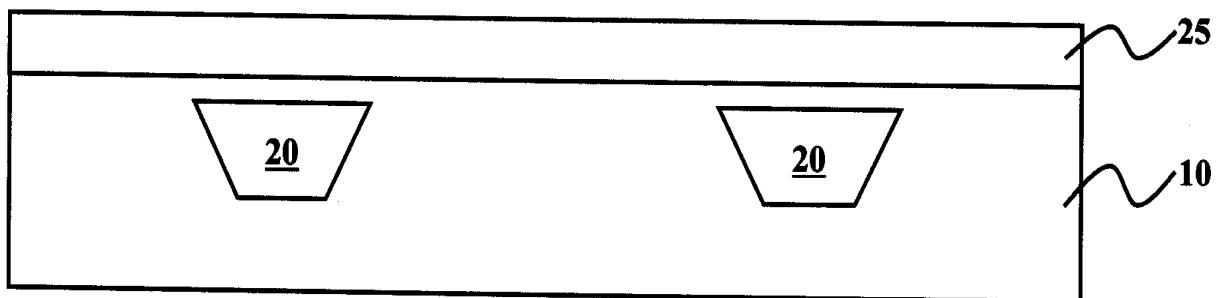


Figure 1(f)

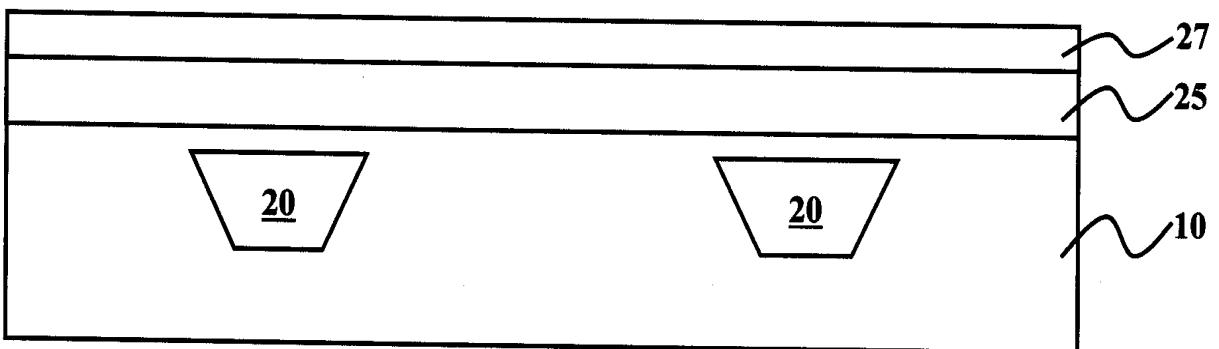


Figure 1(g)

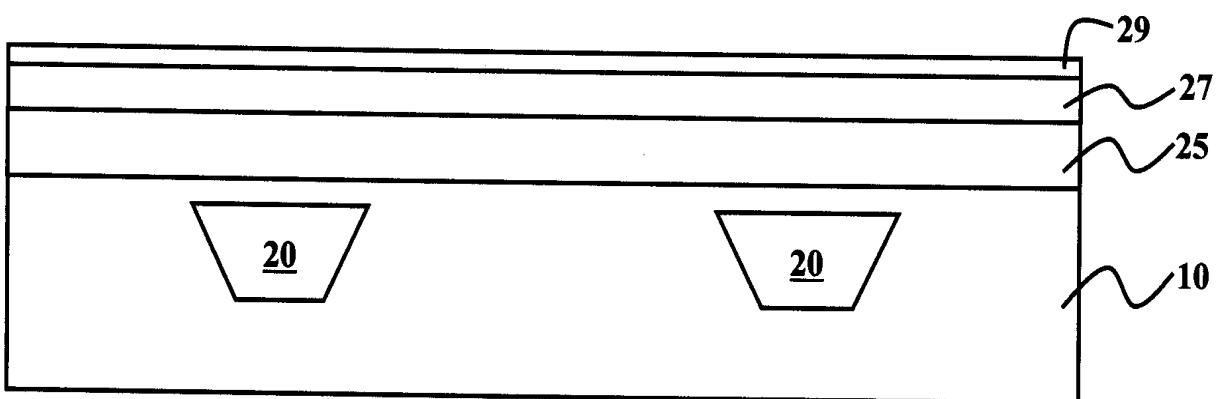


Figure 1(h)

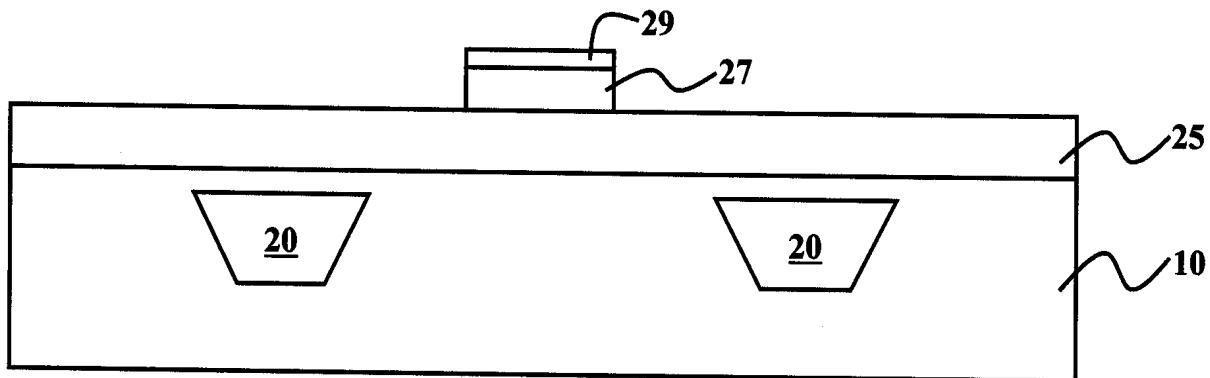


Figure 1(i)

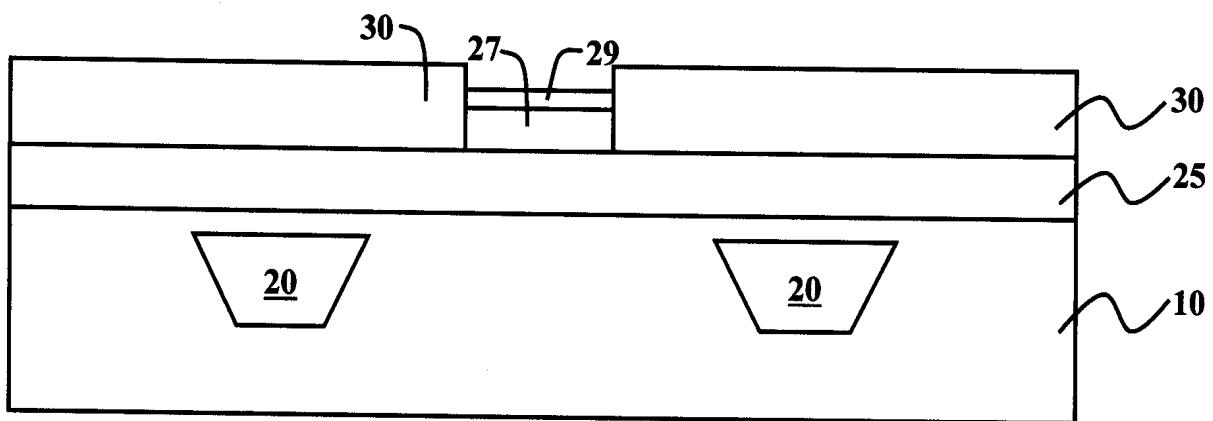


Figure 1(j)

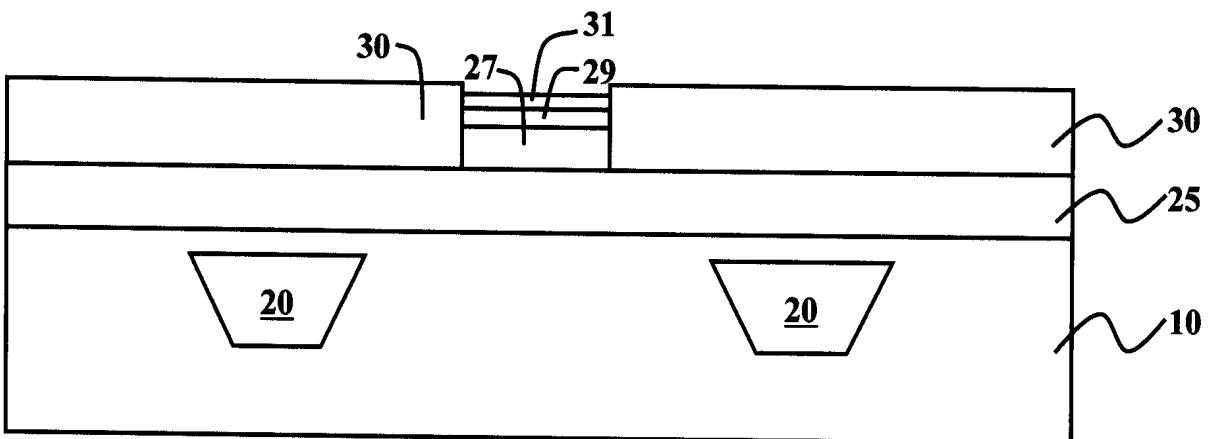


Figure 1(k)

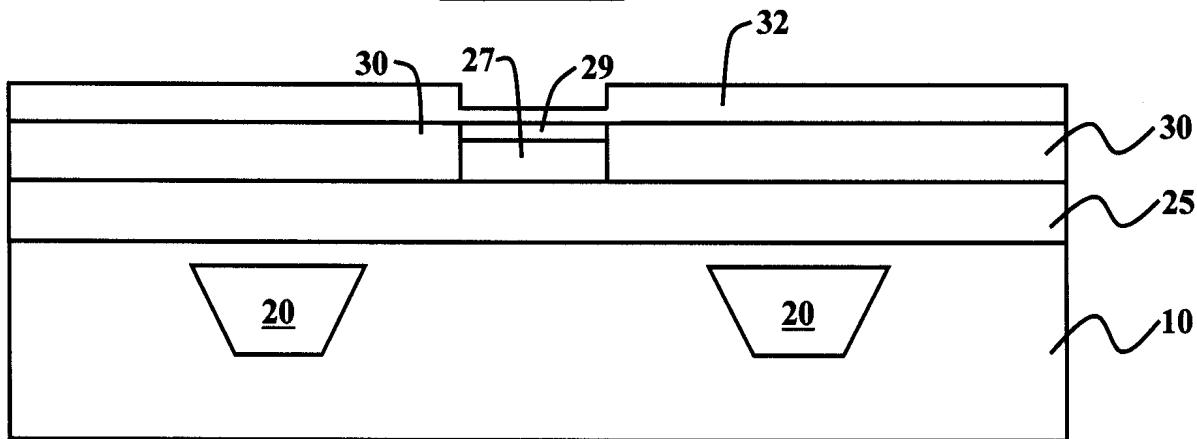


Figure 1(l)

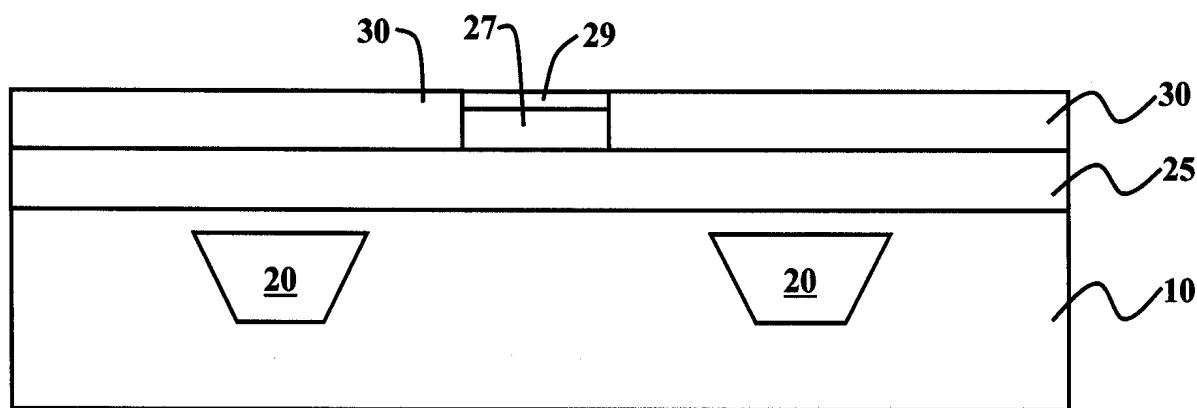


Figure 1(m)

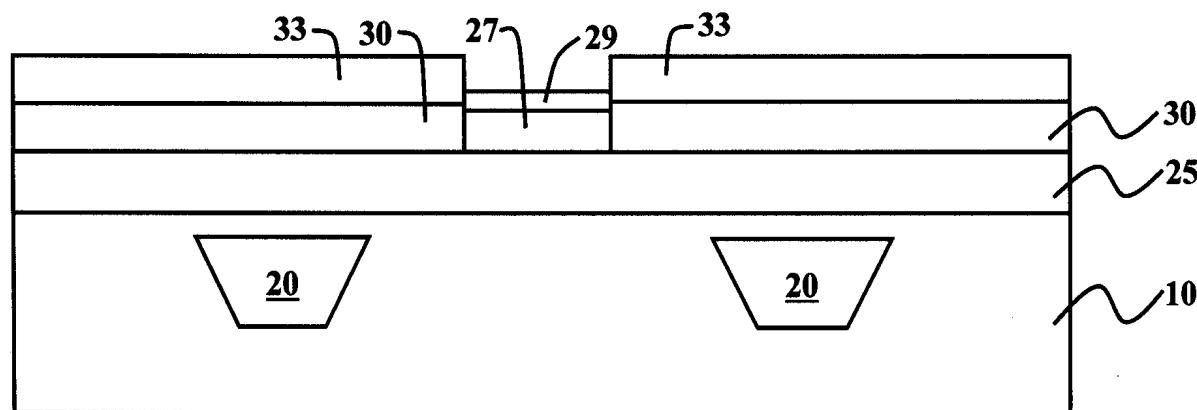


Figure 1(n)

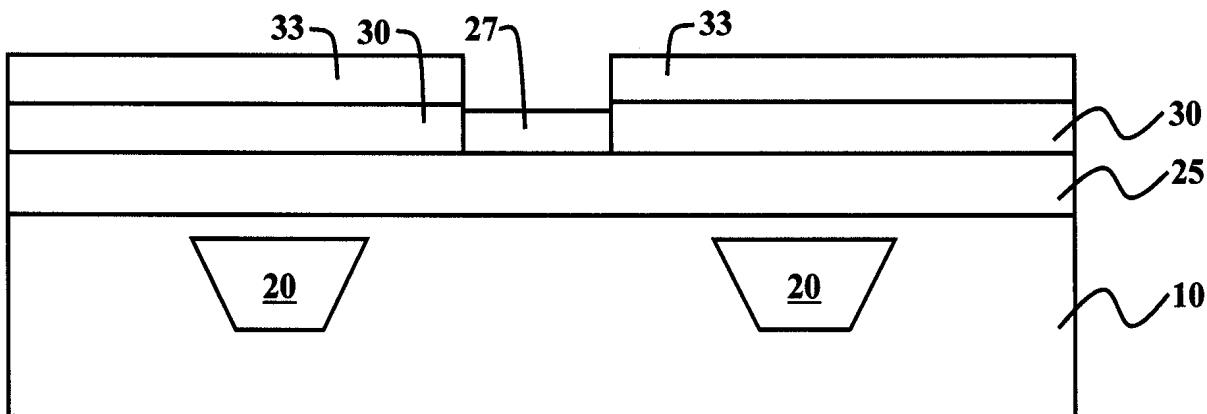


Figure 1(o)

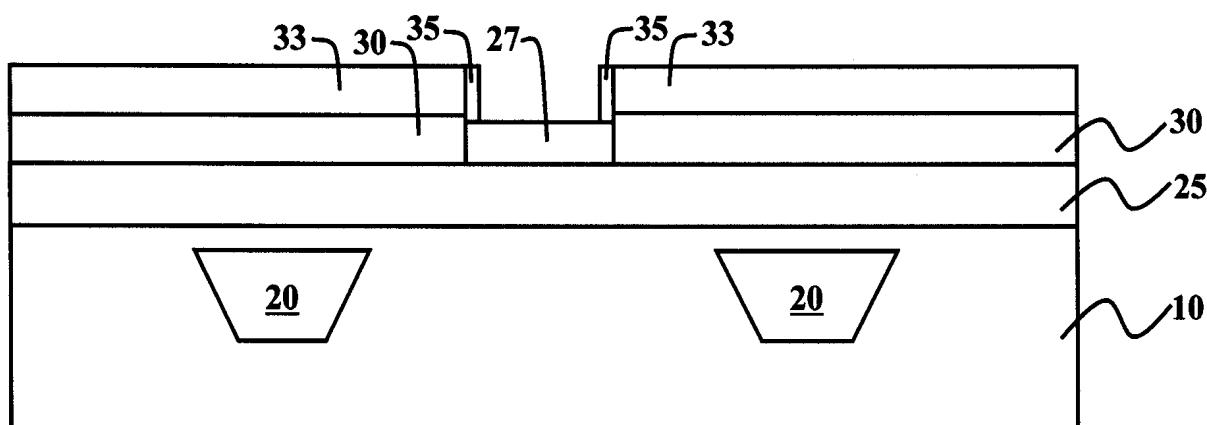


Figure 1(p)

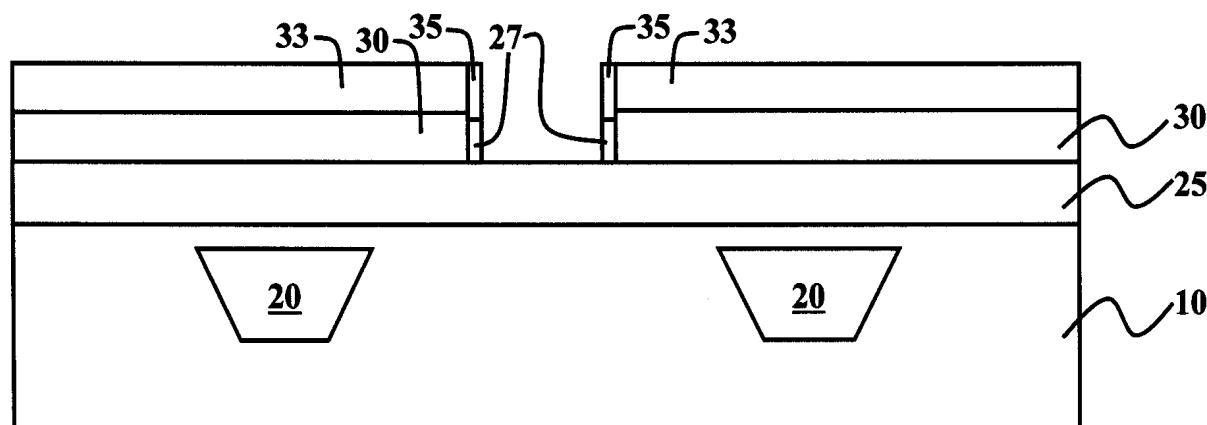


Figure 1(q)

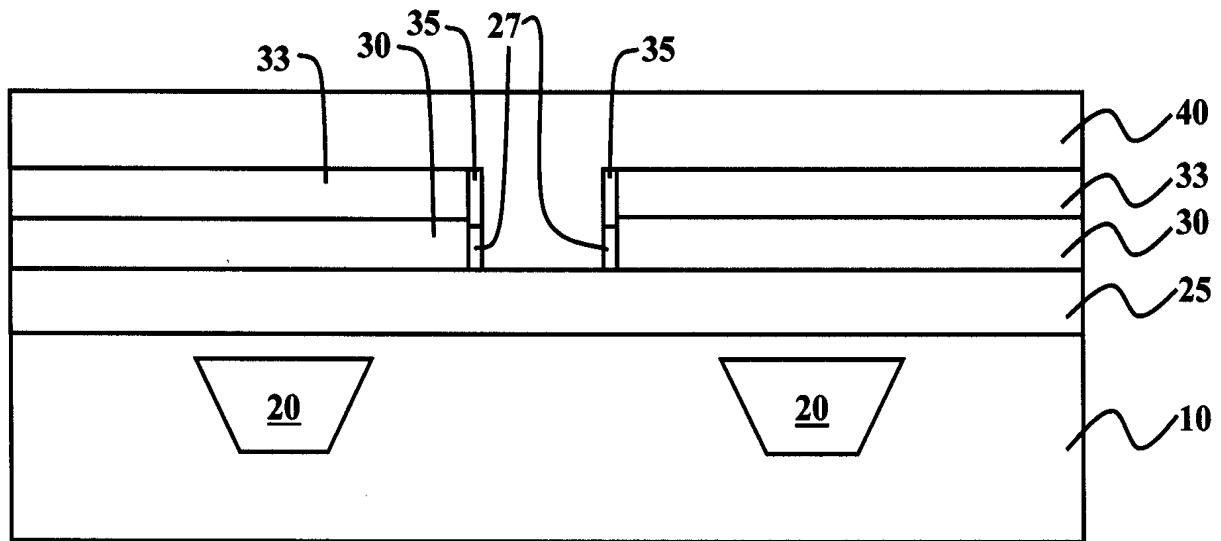


Figure 1(r)

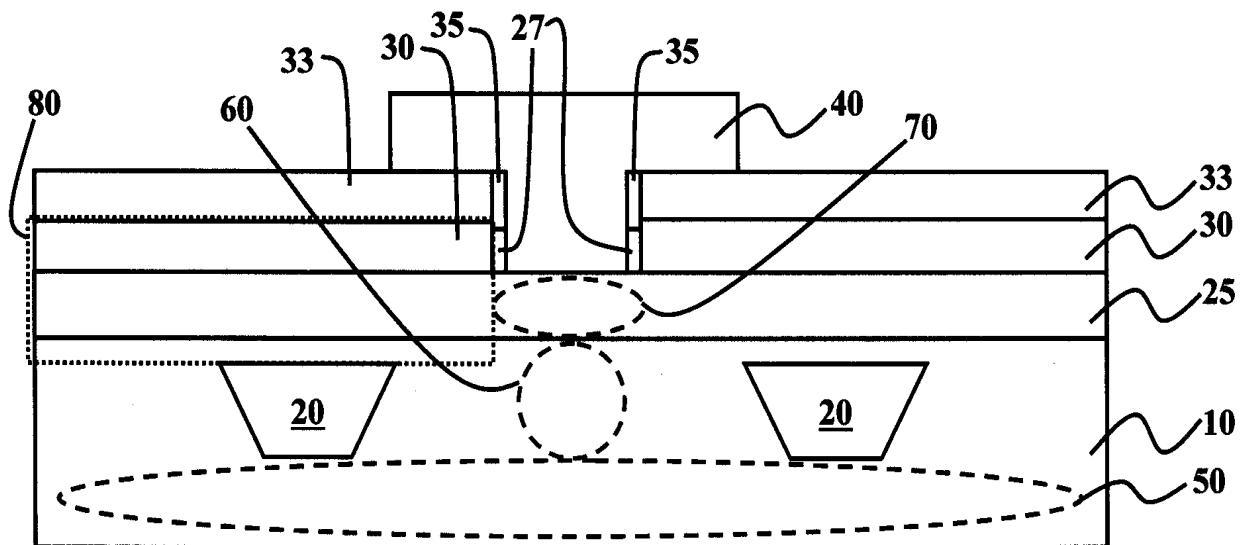


Figure 2(a)

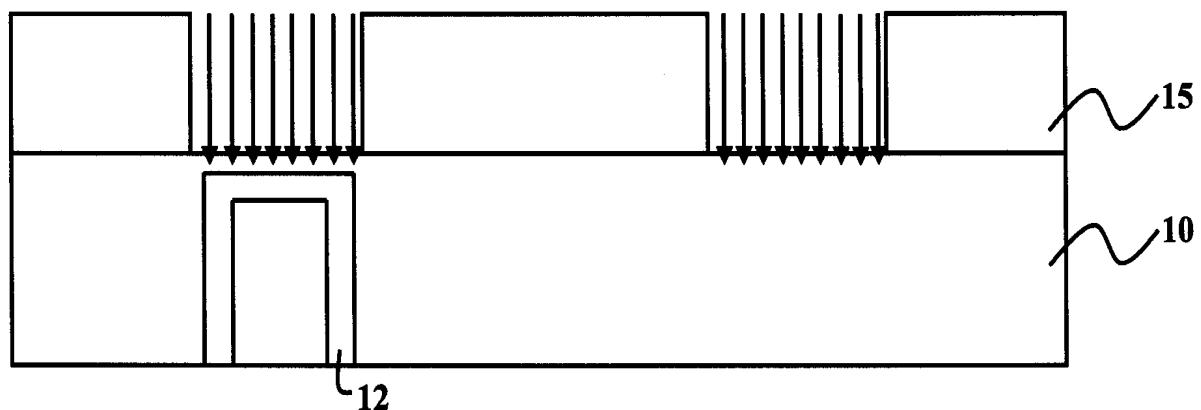


Figure 2(b)



Figure 3(a)

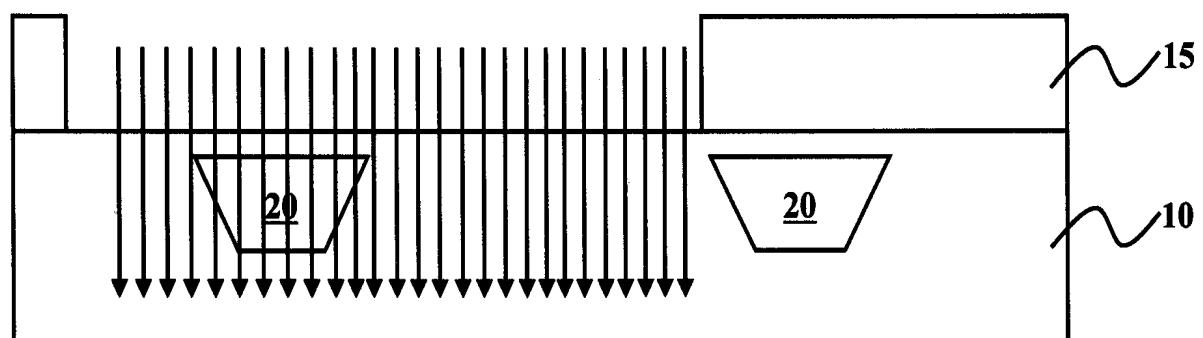


Figure 3(b)

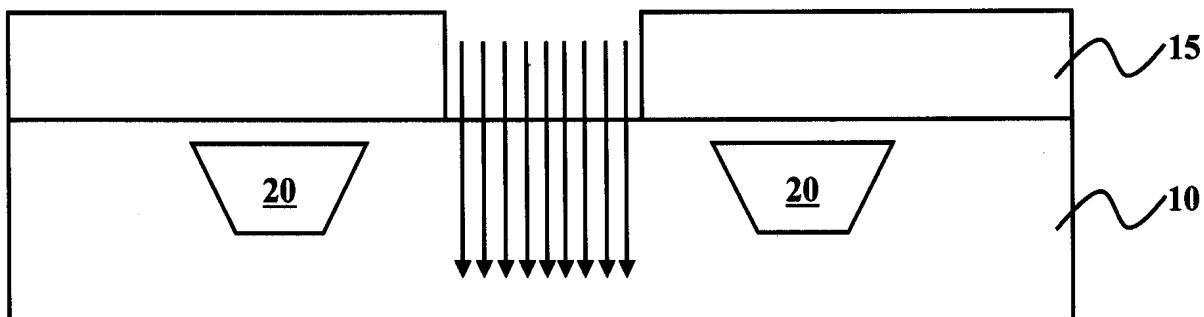


Figure 4(a)

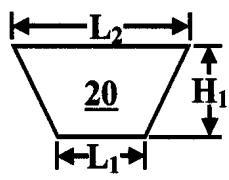


Figure 4(b)

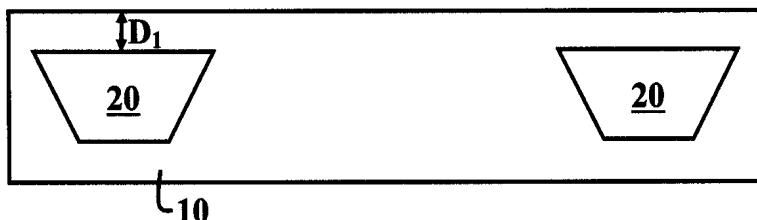


Figure 5(a)

Forming an isolation region below an upper surface of a semiconductor substrate.

500

Forming a single crystal extrinsic base on an upper surface of the isolation region.

502

Forming single crystal intrinsic base over the semiconductor substrate.

504

Figure 5(b)

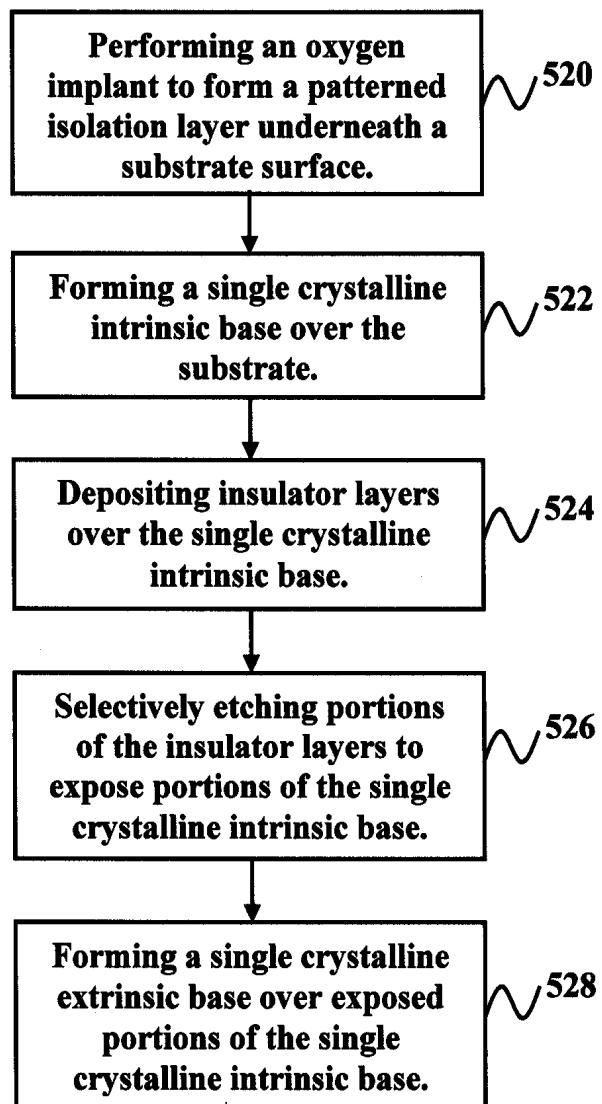


Figure 5(c)

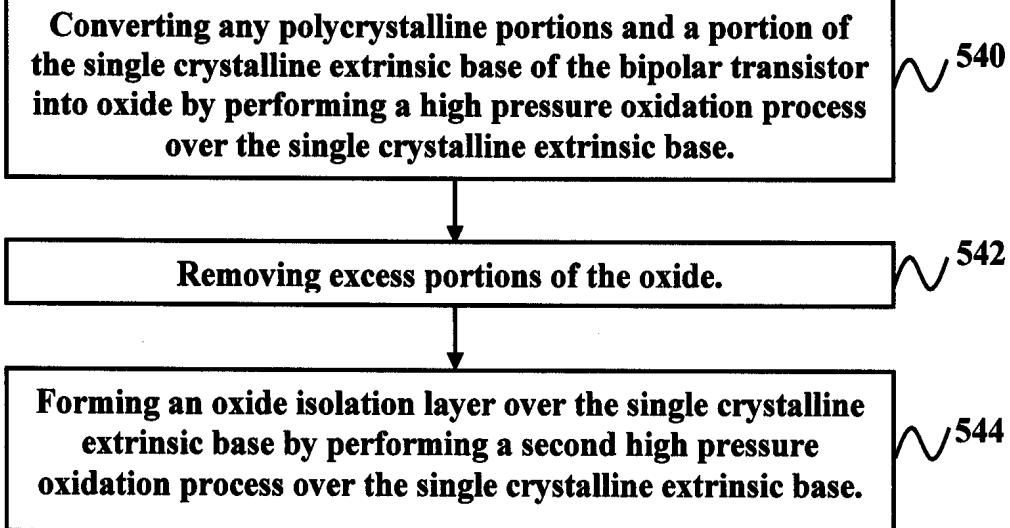


Figure 5(d)

